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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: Not yet assigned
Examiner: Not yet assigned

In Re PATENT APPLICATION OF

Applicant(s) : John P. DEVALE et al.

Appln. No. : 10/747,625

Filing Date : December 30, 2003

For : PREDICTIVE FILTERING OF REGISTER CACHE ENTRY

Atty. Dkt. : 42339-193266

INFORMATION DISCLOSURE STATEMENT

26694
U.S. PATENT AND TRADEMARK OFFICE

May 7, 2004

MAIL STOP DD
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an Information Disclosure Statement submitted under 37 C.F.R. § 1.97 within the time specified under 37 C.F.R. § 1.97(b).

Enclosed please find the attached PTO-1449 and copies of the cited documents therein, listing references referenced in the above-identified application.

In order to comply with applicant's duty of disclosure under 37 C.F.R. § 1.97, the U.S. Patent Office is notified of the documents which are listed on the attached Form PTO-1449 and which the Examiner may deem relevant to patentability of the claims of the above-identified application. One copy of each of the listed documents is submitted herewith.

The present Information Disclosure Statement is being filed before the mailing date of the first Office Action on the merits, and therefore no Statement Under 37 C.F.R. § 1.97(e) or fee under 37 C.F.R. § 1.17(p) is required.

In view of the above, no further translation or statement of relevance is required, and as all requirements of 37 C.F.R. § 1.97 and all official guide lines pertaining to Information Disclosure Statements have been complied with, and it is therefore respectfully requested that the Examiner consider the documents and make them of record.

Respectfully submitted,

Date: May 7, 2004

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/747,625
Filing Date	December 30, 2003
First Named Inventor	John P. DEVALE
Group Art Unit	Not yet assigned
Examiner Name	Not yet assigned
Attorney Docket Number	42339-193266

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OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1	Balasubramonian, R., et al. "Reducing the Complexity of the Register File in Dynamic Superscalar Processors." *Proc. of the 34th Int. Symposium on Microarchitecture (MICRO34)*, Dec. 2001.	
	2	Brekelbaum, N., et al., "Hierarchical Scheduling Windows." *Proc. of the 35th Int. Symposium on Microarchitecture (MICRO35)*, Nov. 2002.	
	3	Cruz, K. et al., "Multiple-banked Register File Architectures." *Proc. Of the Int. Symposium on Computer Architecture*, Jun. 2000.	
	4	Gonzalez, A., et al., "Virtual-physical registers." Proc. *of the 4th Int. Symposium on High Performance Computer Architecture*, Feb. 1998.	
	5	Hinton, G., et al., "The Microarchitecture of the Pentium 4® Processor." *Intel Technical Journal*, Q1 2001, pp. 1-13.	
	6	"Intel® Itanium® Architecture Software Developer's Manual." Intel Corporation 2002.	
	7	Jiménez, D. and C. Lin, "Dynamic Branch Prediction with Perceptrons," *Proc. of the 7th Int. Symposium on High Performance Computer Architecture (HPCA)*, 2001.	
	8	Kim, I. and Lipasti, M., "Half-Price Architecture." *Proc. of the Intl. Symposium on Computer Architecture*, 2003.	
	9	Kim, N., and Mudge, T., "Reducing Register Ports Using Delayed Write-Back Queues and Operand Pre-Fetch." *International Conference on Supercomputing*, 2003.	
	10	Kumar, R., "Scalable register file organization for a multiple issue microprocessor." *I.E.E. Electronics Letters*, Vol. 32, No. 7, 28 March 1996, pp. 634-636.	
	11	Park. I., et al. "Reducing Register Ports for Higher Speed and Lower Energy, " *Proc. of the 35th int. Symposium on Microarchitecture (MICRO35)*, Nov. 2002.	
	12	Postiff, M., et. al., "Integrating Superscalar Processor Components to Implement Register Caching." *International Conference on Supercomputing*, 2001.	
	13	Seznec. A., et al., "Register Write Specialization Register Read Specialization: A Path to Complexity-Effective Wise-Issue Superscalar Processors." *Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture*, 2002, pp. 1-12.	
	14	Shivakumar, P., et al., "An Integrated Cache Timing, Power, and Area Model," *WRL Research Report*, Feb. 2002.	
	15	Tseng, J. and K. Asanovic, "Banked Multiported Register Files for High-Frequency Superscalar Microprocessors." *Proc. Of the Intl. Symposium on Computer Architecture*, 2003.	
	16	Yung, R. and Wilhelm, N., "Caching Processor General Registers." *In Proceedings of the International Conference on Circuits Design*, 1995, pp. 307-312.	
	17	Borch, E., Manne, S., Emer, J., Tune, E., "Loose Loops Sink Chips." *The Proceedings of the 8th Int. Symp. on High Performance Computer Architecture*, 2002, pp. 1-12.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Unique citation designation number. [2] See attached Kinds of U.S. Patent Documents. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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